IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| Applicant | : | Marc Blumer |
| Application No. | : | 10/642,419 |
| Filed | : | 15 August 2003 |
| For | : | DIGITAL SPREAD SPECTRUM SIMULATOR |
| Group Art Unit | : | 2611 |
| Examiner | : | JAISON JOSEPH |

Mail Stop AMENDMENT
Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

DECLARATION OF MARC BLUMER
PURSUANT TO 37 C.F.R. § 1.131

1. My name is Marc Blumer. I am over eighteen years of age and am otherwise competent to make this declaration. All facts stated herein are based on my personal knowledge.

2. I am presently employed by Electronics for Imaging, Inc., ("EFI") assignee of the above-identified patent application. I have been employed by EFI since March 16, 1992.

3. I am the inventor of the subject matter disclosed in above-identified patent. I have reviewed and understand the contents of the application and the March 21, 2007 Final Office Action for this application.

4. I disclosed the subject matter of this application well before November 12, 1999. Copies of several invention disclosures are attached hereto as Exhibits A, B and C. The dates of each of the documents are well before November 12, 1999.

5. Before November 12, 1999, I reduced the invention to practice. Exhibits A, B and C each include diagrams of circuits for generating a reduced amplitude clock pulse. In particular, each of the circuits (a) receives a clock signal; (b) generates a delayed clock signal based on the clock signal; (c) provides a multiplexer having a first input adapted to receive the clock signal, a second input adapted to receive the delayed clock signal, and a third input used to selectively couple the first and second inputs to a multiplexer output; and (d) provides a state machine having an output coupled to the third input of the multiplexer, the state machine adapted to cause the multiplexer to sequentially couple the first and second inputs to the multiplexer output.

6. I declare that all statements made herein of my own knowledge are true and correct, and that all statements made on information and belief are believed to be true, and further that I have made these statements with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity and/or enforceability of this application or any patent that may issue thereon.

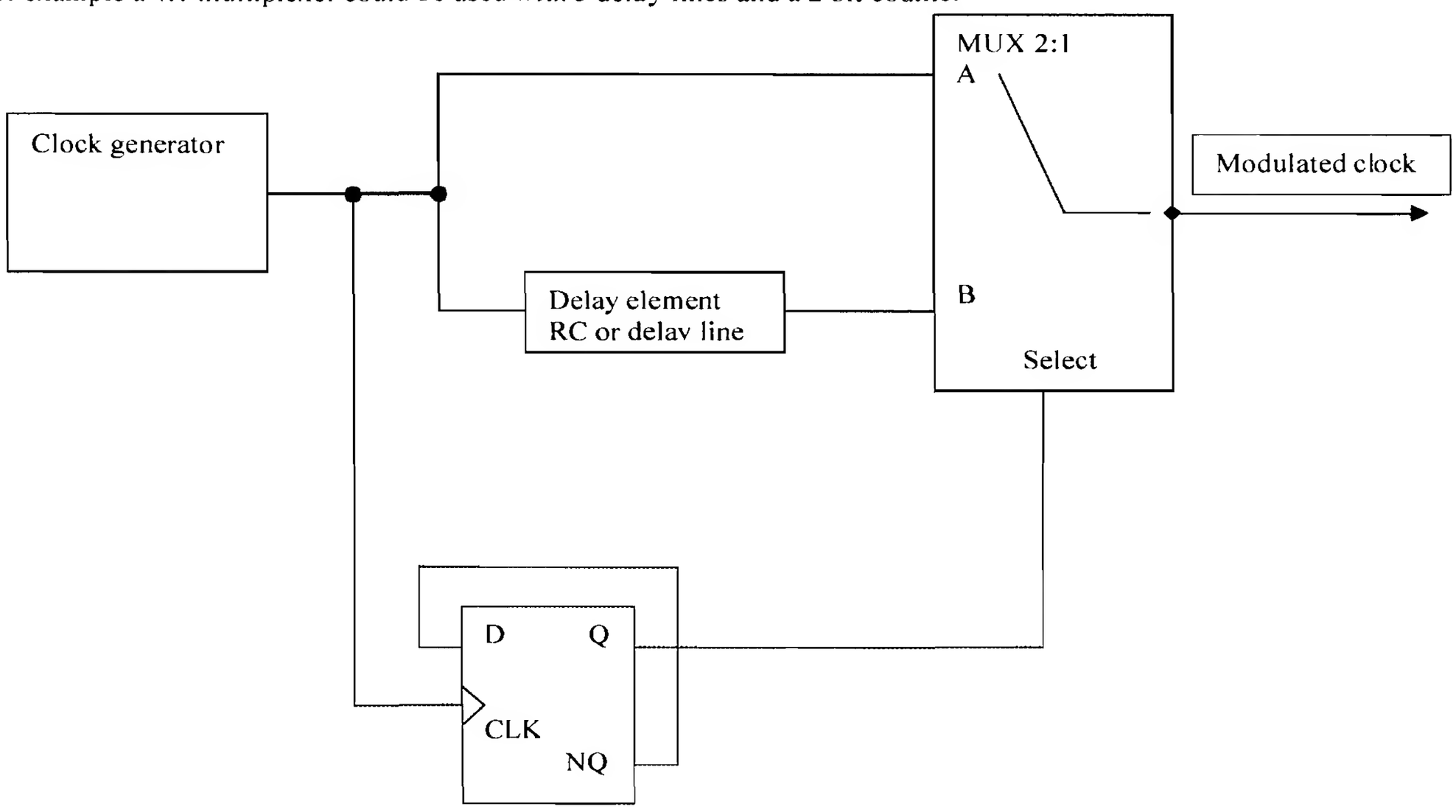
Executed this 11th day of July 2007.

Marc Blumer

EXHIBIT A

# LOW COST SPREAD SPECTRUM MODULATOR

This is a slightly modified version of what I showed last time. It is more generic in the sense that there is no restriction on how to to delay. RC or delay line is fine.
It consists of an oscillator driving a 2 to 1 multiplexer directly or through a delay line alternatively.
The output of the multiplexer produces two different frequencies.
There is no limit to the number of frequencies generated.
For example a 4:1 multiplexer could be used with 3 delay lines and a 2 bit counter



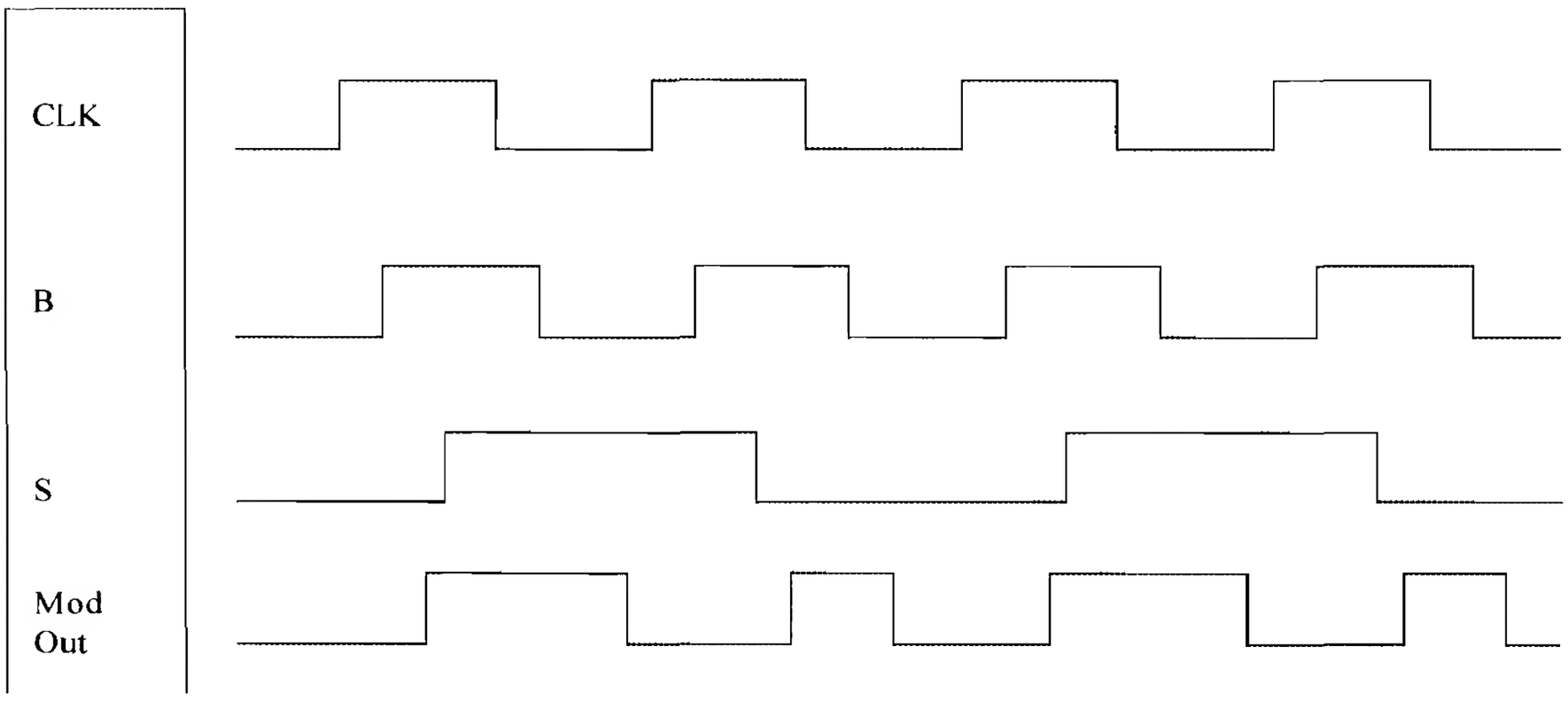



EXHIBIT B

# LOW COST SPREAD SPECTRUM MODULATOR

This is a slightly modified version of what I showed last time. It is more generic in the sense that there is no restriction on how to to delay. RC or delay line is fine.
Using a standard spread spectrum modulator to reduce EMI interference is not only costly but does not work for all print engines. Some of the print engines provide a video clock that can be turned on before a document is printed and turned off again after the last page instantaneously. A standard PLL based spread spectrum modulator cannot cope with turning on and off the clock input. The idea is to have a low cost system that can be instantly turned on and off. The system proposed will only work in a system tolerant to jitter.
It consists of an oscillator driving a n to 1 multiplexer directly or through n-1 delay lines alternatively.
By selecting the different delays as a suite in the following manner:
T1=1, T2=1+2, T3=1+2+3 etc..., the number of different frequencies is maximized. For example with 3 delay lines, T1=1, T2=3, T3=6, you obtain the following clock periods: T, T+1, T+2, T+3, T+5, T+6, T-1, T-2, T-3, T-5, T-6. By selecting only three delay lines, 4*4-4=11 different frequencies have been generated, reducing the spectral noise. By having 4 delay lines, 5*5-6=19 frequencies are generated, 5 delay lines, 6*6-8=28 frequencies etc...
The output of the multiplexer produces n different frequencies.
There is no limit to the number of frequencies generated.

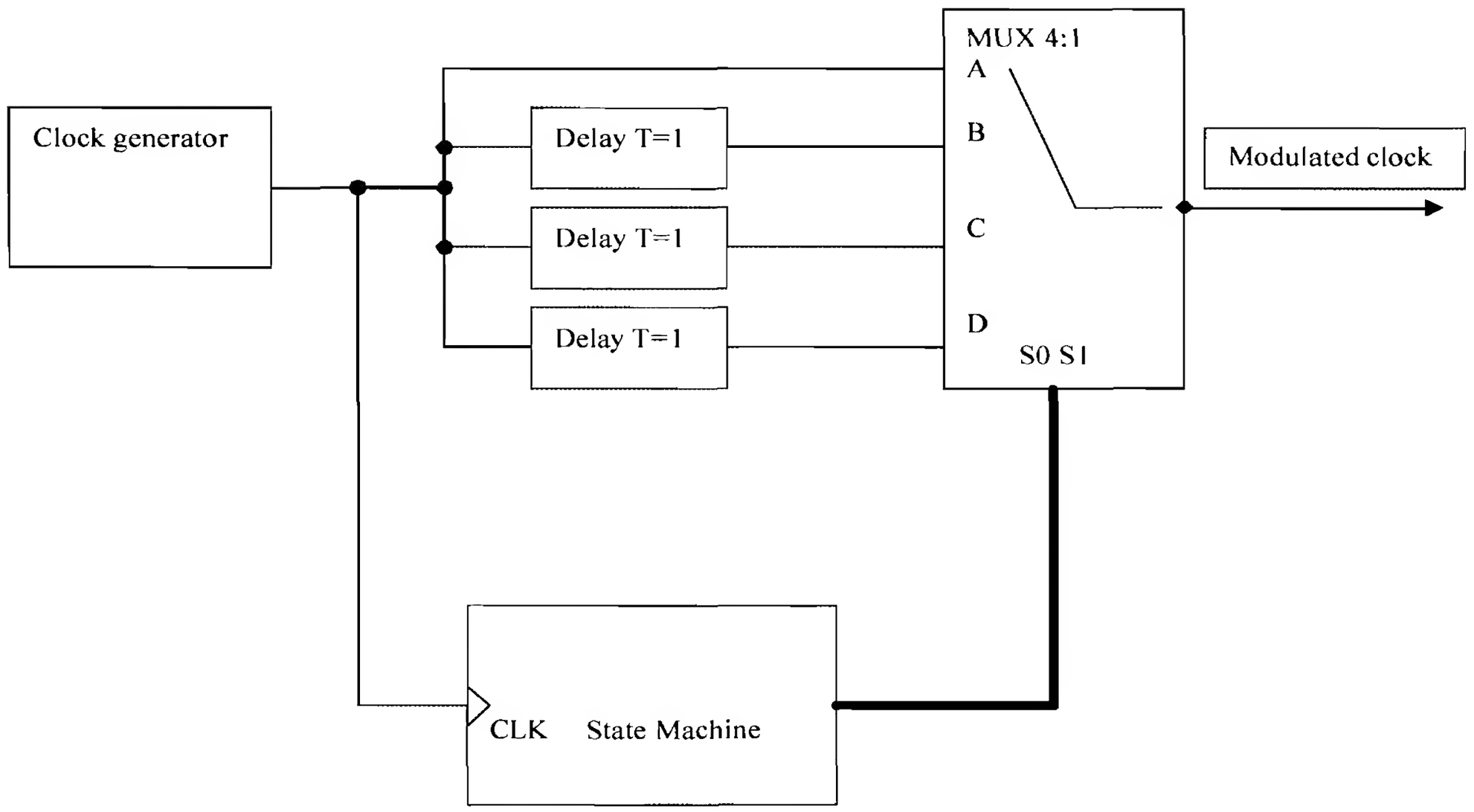



**Fig 1 Block diagram with 3 delays**

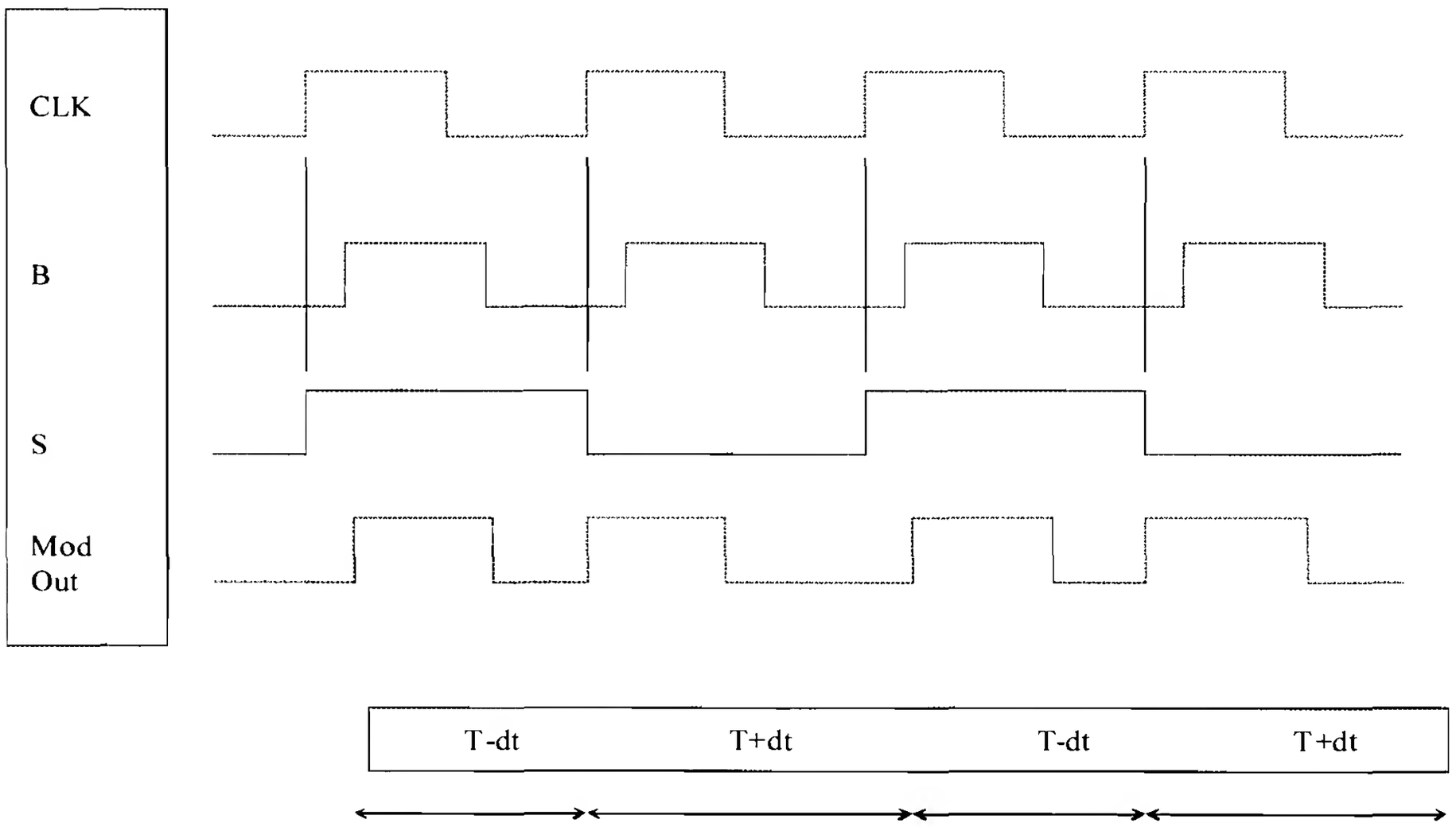


**Fig 2 Timing diagram with only one delay line**

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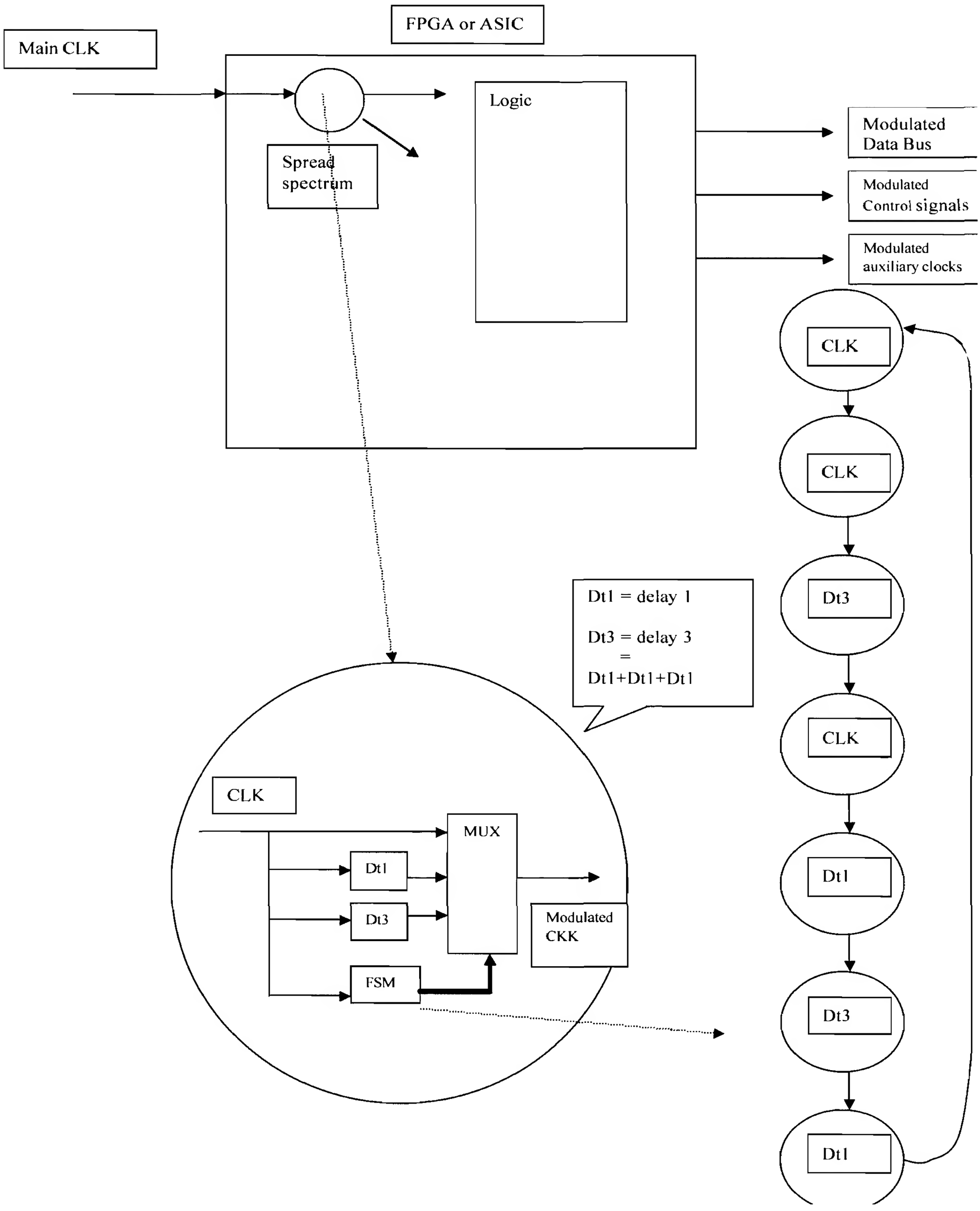
# EXHIBIT C


FPGA or ASIC
Main CLK
Logic
Spread spectrum
Modulated Data Bus
Modulated Control signals
Modulated auxiliary clocks
CLK
CLK
Dt3
CLK
Dt1 = delay 1
Dt3 = delay 3 = Dt1+Dt1+Dt1
CLK
MUX
Dt1
Dt3
FSM
Modulated CKK
Dt1
Dt3
Dt1